

JEDEC STANDARD

Electrostatic Discharge (ESD) Sensitivity Testing – Reporting ESD Withstand Levels on Datasheets

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ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – REPORTING ESD WITHSTAND LEVELS ON DATASHEETS

CONTENTS

Introduction	ii
1 Scope	1
2 Referenced publications	1
3 Definitions	1
4 General Considerations	2
5 Simple ESD Data format	3
5.1 Standard Test Method Citation	3
5.2 Device Withstand Threshold.....	3
5.3 Device Classification	3
6 Additional Information options and examples	4
Annex A (Informative): HBM and CDM Classification Levels.....	5
Annex B (Informative): Examples of Entry of Exception Data.....	6

TABLES

Table 1: Simple Representation of ESD Data.....	3
Table 2: HBM Classification Levels (ANSI/ESD/JEDEC JS-001-2017)	5
Table 3: CDM Classification Levels (ANSI/ESD/JEDEC JS-002-2018)	5
Table 4: Inclusion of Lower ESD Level High-Speed Pin Data	6
Table 5: Expressing Exceptions in Terms of Targets.....	6

ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – REPORTING ESD WITHSTAND LEVELS ON DATASHEETS

Introduction

This document is intended to guide device manufacturers in developing datasheets and to device customers in understanding datasheet entries. Standardized ESD stress test methods have been developed to evaluate the relative sensitivity of devices. Although these methods are available, the results of the testing are not always provided by the suppliers, especially charged device model (CDM) levels. The document provides a standardized template which includes a minimum information set and gives guidelines for expanded individual pin information when needed. The document should improve the availability and usefulness of reported ESD data.

ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – REPORTING ESD WITHSTAND LEVELS ON DATASHEETS

(From JEDEC Bod Ballot JCB-204-34, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This document applies to ESD withstand level information in datasheets or other information publications such as reliability or qualification reports. All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) should have this information provided.

NOTE This document does not apply to electrically-initiated explosive devices, flammable liquids, or powders.

2 Referenced Publications

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this document to the extent specified herein:

ANSI/ESDA/JEDEC JS-001, *Human Body Model (HBM) – Component Level*^{1,2}

ANSI/ESDA/JEDEC JS-002, *Charged Device Model (CDM) – Device Level*^{1,2}

ESD ADV1.0, *Glossary of Terms*²

IEC 61000-4-2, *Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*³

JEDEC JESD47, *Stress-Test Driven Qualification of Integrated Circuits*²

3 Definitions

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, EOS/ESD Association, Inc.'s Glossary of Terms available for complimentary download at www.esda.org.

ESD withstand level. The highest voltage level that does not cause device failure; the device passes all tested lower voltage levels.

¹ EOS/ESD Association, Inc., 7900 Turin Road, Bldg. 3, Rome, NY 13440; Ph: 315-339-6937; www.esda.org

² JEDEC, 3103 North 10th Street, Arlington, VA 22201; Ph: 703-907-7534; www.jedec.org

³ IEC – International Electrotechnical Commission, www.iec.ch

4 General Considerations

There are several important points to consider when using this document, either to develop datasheets or in reading datasheets.

- The standard test methods used, including version, should be cited. In most cases, these will be ANSI/ESDA/JEDEC JS-001-20xx (HBM) and ANSI/ESDA/JEDEC JS-002-20yy (CDM). Other standards from accredited standards bodies may also be used.
- Complete ESD handling characterization of devices requires BOTH HBM and CDM as specified in JEDEC JESD 47.
- It is not sufficient to report data as “ESD” without the specific ESD standard designations for both models.
- The HBM and CDM data provided by the test methods are intended to provide relative, standardized figures of merit for sensitivity to these types of ESD during manufacturing, test, repair and any process where sensitive devices are subject to handling by people or production equipment in an ESD protected area.
- HBM and CDM withstand thresholds are relevant only to device handling. These ratings do not predict and are not relevant to performance in system-level tests such as IEC 61000-4-2.
- Performance levels determined using methods intended to simulate system-level performance (for example, IEC 61000-4-2 ESD gun) is not relevant to handling and should not be listed as “HBM” levels in datasheets. Reporting system-level test data is outside the scope of this document since it does not address handling in an ESD protected area (EPA).
- Using the JS-001 HBM network values ($C=100\text{ pF}$, $R=1500\text{ ohm}$) in a system-level ESD gun is not sufficient to produce a valid device-level HBM test.

5 Simple ESD Data Format

Table 1 is a suggested format for presenting ESD withstand levels. In most cases, this simple representation is sufficient as long as both ESD model results are included.

Table 1 — Simple Representation of ESD Data

ESD Information for Handling of ESDS in an ESD Protected Area
CDM (ANSI/ESDA/JEDEC JS-002-2014): [enter withstand level (e.g., 250 volts) and/or alphanumeric classification (for example, C1)] NOTE [enter any significant test details or exceptions here]
HBM (ANSI/ESDA/JEDEC JS-001-2017): [enter withstand level (e.g., 250 volts) and/or alphanumeric classification (for example, 1A)] NOTE [enter any significant test details or exceptions here]

5.1 Standard Test Method Citation

It is important to list the relevant standard, including version number (publication year), so that the details of the stress waveform and pin or pin combinations stressed can be understood. If there are any unique exceptions to the use of the standard, a note should be used to highlight the exception.

5.2 Device Withstand Level

By definition, the lowest performing pin (CDM) or pin combination (HBM) determines these numerical values. Both HBM and CDM levels should be reported.

5.3 Device Classification

Some device users prefer to use a device classification designation which represents a threshold voltage range. These ranges are defined in the cited CDM and HBM test method standards and are also in Annex A. It is also recommended to report the withstand levels when reporting the device classification designation.

6 Additional Information Options and Examples

The manufacturer may want to provide clarifying data and stressing information that will give the device user better insight into how to handle the device. This information may include identification of the most sensitive pins or information about relative ESD risk. Suggested ways of presenting this information are:

- List results pin-by-pin. (May only be practical for a low-pin-count device)
- List results by pin groups. (for example, I/O and Power/Ground)
- List exceptions – Useful when a small number of pins cause a low threshold. An indication of the percentage of pins that do not meet the desired level may also be useful.
- List as an exception to a “target” performance – Similar to above except the baseline is a “target” level which is an expected level of performance for a device family, technology or application (See Table 5)
- Any other relevant data to indicate risk (or lack of risk) in an EPA

Annex B provides some examples.

Annex A (informative) – HBM and CDM classification levels

These tables were from the current document versions at the time of publication of this document. For the most recent information, the user should consult the latest versions of JS-001 and JS-002.

Table 2 — HBM Classification Levels (ANSI/ESDA/JEDEC JS-001-2017)

Classification	Voltage Range (V)
0Z	< 50
0A	50 to < 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C*	1000 to < 2000
2*	2000 to < 4000
3A*	4000 to < 8000
3B*	≥ 8000

Table 3 — CDM Classification Levels (ANSI/ESDA/JEDEC JS-002-2018)

Classification Level	Classification Test Condition (in volts)
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1000
C3	≥ 1000

Annex B (Informative) – Examples of entry of exception data

In most cases, the ESD data sheet entries will be simple as indicated in Table 1. However, in some cases, the supplier may want to include additional information, such as when a device has a lower than expected or desired threshold due to a few “exception” pins. The description of exception pins may be done in any manner which accurately reflects the pins ESD performance. Table 4 and Table 5 give examples of how this information might be presented concisely in a data sheet. These examples are not intended to exclude other ways of providing information. In some cases, suppliers and users may collaborate on the best way to present this additional data.

Table 4 and Table 5 present two possible ways of expressing the same hypothetical situation: A 20-pin device has been evaluated using ANSI/ESDA/JEDEC JS-002 and ANSI/ESDA/JEDEC JS-001. 18 of the 20 pins pass CDM at 500 volts while two high-speed pins (here designated as pins 3 and 4) only pass 250 volts. Similarly, 18 of the pins pass HBM at 1000 volts while the same high-speed pins (3 and 4) only pass 500 volts. Table 4 describes one way of conveying these results on a datasheet.

Table 4 — Inclusion of Lower ESD Level High-Speed Pin Data

ESD Information for Handling of ESDS in an ESD Protected Area
CDM (ANSI/ESDA/JEDEC JS-002-2014): CDM Withstand Threshold 250 volts; CDM Class C1 NOTE The CDM withstand threshold is determined by two high-speed pins (3 and 4) which pass 250 volts. All other pins pass 500 volts.
HBM (ANSI/ESDA/JEDEC JS-001-2017): HBM Withstand Threshold 500 volts; HBM Class 1B NOTE The HBM withstand threshold is determined by two high-speed pins (3 and 4) which pass 500 volts. All other pins pass 1000 volts.

In some cases, suppliers and users prefer the information to be expressed in terms of “target levels” for a given family of devices or a given technology. In these cases, Table 5 illustrates a description of low-threshold, high-speed pins.

Table 5 — Expressing Exceptions in Terms of Targets

ESD Information for Handling of ESDS in an ESD Protected Area
CDM (ANSI/ESDA/JEDEC JS-002-2014): CDM Withstand Threshold 250 volts; CDM Class C1 NOTE The target CDM threshold for this device family is 500 volts and 18 out of 20 pins pass this level. The 250-volt CDM level of pins 3 and 4 determines the overall device threshold. This lower level is required to meet the functional performance requirements of these high-speed pins.
HBM (ANSI/ESDA/JEDEC JS-001-2017): HBM Withstand Threshold 500 volts; HBM Class 1B NOTE The target HBM threshold for this device family is 1000 volts and 18 out of 20 pins pass this level. The 500-volt HBM level of pins 3 and 4 determines the overall device threshold. This lower level is required to meet the functional performance requirements of these high-speed pins.



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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

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